TS5A3159 1-Ω SPDT Analog Switch

1 Features

- Specified Break-Before-Make Switching
- Low ON-State Resistance (1 Ω)
- Control Inputs are 5-V Tolerant
- Low Charge Injection
- Excellent ON-Resistance Matching
- Low Total Harmonic Distortion
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Mobile Phones
- Consumer and Computing
- Portable Instrumentation

3 Description

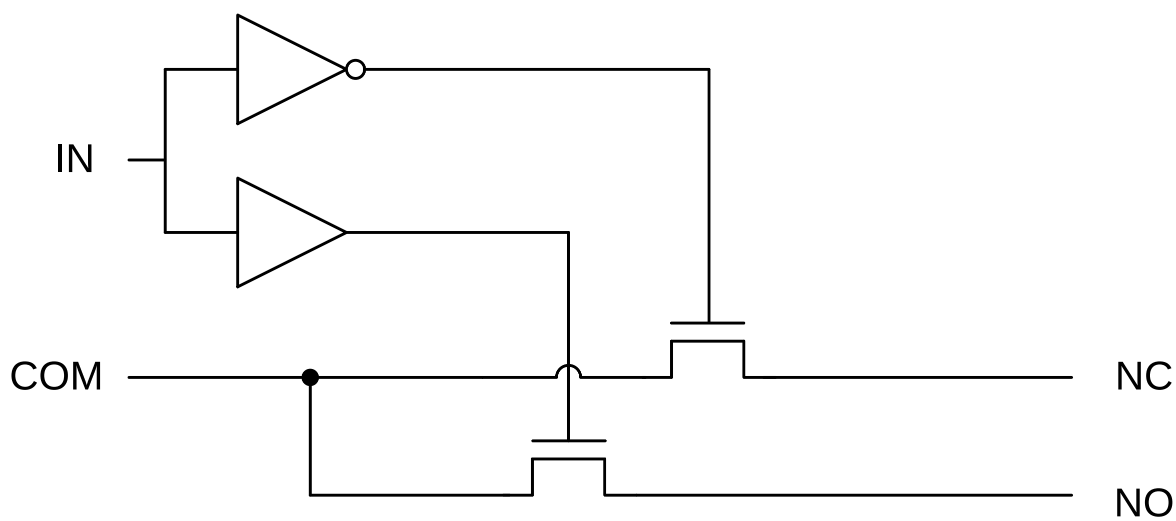
The TS5A3159 device is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance and an excellent ON-state resistance matching, with the break-before-make feature to prevent signal distortion during the transferring of a signal from one channel to another. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A3159	SOT-23 (6)	2.90 mm × 1.60 mm
	SC70 (6)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2015) to Revision D — **Page**

- Changed NO Pin description 3
- Deleted Added Junction temperature to the Absolute Maximum Ratings table. 3

Changes from Revision B (September 2004) to Revision C — **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1

Changes from Revision A (September 2004) to Revision B — **Page**

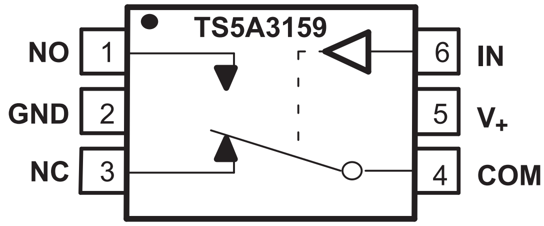
- Removed *Ordering Information* table. 1

Changes from Original (August 2004) to Revision A — **Page**

- Corrected Figure 11 graphic 12

5 Pin Configuration and Functions

DBV and DCK Packages
6-Pin SOT-23 and SC-70
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	NO	I/O	Normally open switch port
2	GND	—	Ground
3	NC	I/O	Normally closed switch port
4	COM	I/O	Common switch port
5	V+	—	Power supply
6	IN	I	Switch select. High = COM connected to NO; Low = COM connected to NC.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_+	Supply voltage(2)		–0.5	6.5	V
V_{NO} V_{COM}	Analog voltage(2)(3)(4)		–0.5	V_+ + 0.5	V
$I_{I/OK}$	Analog port diode current	V_{NO}, V_{COM} < 0 or V_{NO}, V_{COM} > V_+		±50	mA
I_{NO} I_{COM}	ON-state switch current	V_{NO}, V_{COM} = 0 to V_+		±200	mA
	ON-state peak switch current(5)			±400	mA
V_{IN}	Digital input voltage(2)(3)		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_{IN} < 0		–50	mA
	Continuous current through V_+ or GND			±100	mA
T_j	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.
(5) Pulse at 1-ms duration < 10% duty cycle.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Switch input/output voltage	0	V_+	V
V+	Supply voltage	1.65	5.5	V
V_I	Control input voltage	0	5.5	V
T_A	Operating temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC[1]		TS5A3159 DBV (SOT-23) 6 PINS	TS5A3159 DCK (SC-70) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165	165	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics for 5-V Supply

V_+ = 4.5 V to 5.5 V and T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP[1]	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{peak}	Peak ON-state resistance	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –30 mA,	Switch ON, see Figure 10	25°C	4.5 V		1	1.5	Ω
				Full				1.5	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 2.5 V, I_{COM} = –30 mA,	Switch ON, see Figure 10	25°C	4.5 V		0.75	1.1	Ω
				Full				1.1	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2.5 V, I_{COM} = –30 mA,	Switch ON, see Figure 10	25°C	4.5 V		0.1		Ω
$r_{on(flat)}$	ON-state resistance flatness	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –30 mA	Switch ON, see Figure 10	25°C	4.5 V		0.233		Ω
		V_{NO} or V_{NC} = 1 V, 1.5 V, 2.5 V, I_{COM} = –30 mA		25°C			0.15		
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO Off leakage current	V_{NC} or V_{NO} = 4.5 V, V_{COM} = 0 V,	Switch OFF, see Figure 11	25°C	5.5 V	–2	0.2	2	nA
				Full		–20		20	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO On leakage current	V_{NC} or V_{NO} = 4.5 V, V_{COM} = Open,	Switch ON, see Figure 12	25°C	5.5 V	–4	2.8	4	nA
				Full		–40		40	
$I_{COM(ON)}$	COM On leakage current	V_{NC} or V_{NO} = 4.5 V or Open, V_{COM} = 4.5 V,	Switch ON, see Figure 12	25°C	5.5 V	–4	0.47	4	nA
				Full		–40		40	
Digital Input (IN)									
V_{IH}	Input logic high			Full		2.4		5.5	V
V_{IL}	Input logic low			Full		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		Full	5.5 V	–1		1	μA

(1) T_A = 25°C.

Electrical Characteristics for 5-V Supply (continued)

V_+ = 4.5 V to 5.5 V and T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Dynamic									
t_{ON}	Turnon time	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, see Figure 14	25°C	4.5 V to 5.5 V		20	35	ns
				Full				40	
t_{OFF}	Turnoff time	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, see Figure 14	25°C	4.5 V to 5.5 V		15	20	ns
				Full				35	
t_{BBM}	Break-before-make time	$V_{NC} = V_{NO} = V_+ / 2$, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	4.5 V to 5.5 V	1	12	14.5	ns
				Full		1			
Q_C	Charge injection	C_L = 1 nF, V_{GEN} = 0 V,	See Figure 19	25°C	5 V		36		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or $V_{NO} = V_+$ or GND,	Switch OFF, see Figure 13	25°C	5 V		23		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or $V_{NO} = V_+$ or GND,	Switch ON, see Figure 13	25°C	5 V		84		pF
$C_{COM(ON)}$	COM ON capacitance	$V_{COM} = V_+$ or GND,	Switch ON, see Figure 13	25°C	5 V		84		pF
C_{IN}	Digital input capacitance	$V_{IN} = V_+$ or GND,	See Figure 13	25°C	5 V		2.1		pF
BW	Bandwidth	R_L = 50 Ω,	Switch ON, see Figure 16	25°C	5 V		100		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see Figure 17	25°C	5 V		–65		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, see Figure 18	25°C	5 V		–65		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, see Figure 20	25°C	5 V		0.01%		
Supply									
I_+	Positive supply current	$V_{IN} = V_+$ or GND,	Switch ON or OFF	Full	5.5 V			0.1	μA

6.6 Electrical Characteristics for 3.3-V Supply

V_+ = 3 V to 3.6 V and T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{peak}	Peak ON-state resistance	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –24 mA,	Switch ON, see Figure 10	25°C	3 V		1.35	2.1	Ω
				Full				2.1	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 2 V, I_{COM} = –24 mA,	Switch ON, see Figure 10	25°C	3 V		1.15	1.5	Ω
				Full				1.5	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –24 mA,	Switch ON, see Figure 10	25°C	3 V		0.11		Ω
$r_{on(flat)}$	ON-state resistance flatness	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –24 mA,	Switch ON, see Figure 10	25°C	3 V		0.225		Ω
		V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –24 mA,		25°C			0.25		

(1) T_A = 25°C.

Electrical Characteristics for 3.3-V Supply (continued)

V_+ = 3 V to 3.6 V and T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP[(1)]	MAX	UNIT
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO Off leakage current	V_{NC} or V_{NO} = 3 V, V_{COM} = 0,	Switch OFF, see Figure 11	25°C	3.6 V		0.2		nA
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO On leakage current	V_{NC} or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, see Figure 12	25°C	3.6 V		2.8		nA
$I_{COM(ON)}$	COM On leakage current	V_{NC} or V_{NO} = 3 V or Open, V_{COM} = 3 V,	Switch ON, see Figure 12	25°C	3.6 V		0.47		nA
Digital Inputs (IN)									
V_{IH}	Input logic high			Full		2		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		Full	3.6 V	–1		1	μA
Dynamic									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 14	25°C	3 V to 3.6 V		30	40	ns
				Full				55	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 14	25°C	3 V to 3.6 V		20	25	ns
				Full				40	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+ / 2, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	3 V to 3.6 V	1	21	29	ns
				Full		1			
Q_C	Charge injection	C_L = 1 nF, V_{GEN} = 0 V,	see Figure 19	25°C	3.3 V		20		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V+ or GND,	Switch OFF, see Figure 13	25°C	3.3 V		23		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch ON, see Figure 13	25°C	3.3 V		84		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND,	Switch ON, see Figure 13	25°C	3.3 V		84		pF
C_{IN}	Digital input capacitance	V_{IN} = V_+ or GND,	See Figure 13	25°C	3.3 V		2.1		pF
BW	Bandwidth	R_L = 50 Ω,	Switch ON, see Figure 16	25°C	3.3 V		100		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see Figure 17	25°C	3.3 V		–65		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, see Figure 18	25°C	3.3 V		–65		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, see Figure 20	25°C	3.3 V		0.015%		
Supply									
I_+	Positive supply current	V_{IN} = V_+ or GND,	Switch ON or OFF	Full	3.6 V			0.1	μA

6.7 Electrical Characteristics for 2.5-V Supply

V_+ = 2.3 V to 2.7 V and T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_+	MIN	TYP[(1)]	MAX	UNIT
Analog Switch								
V_{COM}, V_{NO}, V_{NC}	Analog signal range				0		V_+	V

(1) T_A = 25°C.

Electrical Characteristics for 2.5-V Supply (continued)

V_+ = 2.3 V to 2.7 V and T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
r_{peak}	Peak ON-state resistance	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –8 mA,	Switch ON, see Figure 10	25°C	2.5 V		1.7	2.7	Ω
				Full				2.7	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 1.8 V, I_{COM} = –8 mA,	Switch ON, see Figure 10	25°C	2.5 V		1.45	2	Ω
				Full				2	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 0.8 V, 1.8 V, I_{COM} = –8 mA,	Switch ON, see Figure 10	25°C	2.5 V		0.7		Ω
$r_{on(flat)}$	ON-state resistance flatness	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –8 mA,	Switch ON, see Figure 10	25°C	2.5 V		0.5		Ω
		V_{NO} or V_{NC} = 0.8 V, 1.8 V I_{COM} = –8 mA,		25°C			0.45		
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO Off leakage current	V_{NC} or V_{NO} = 2.3 V, V_{COM} = 0,	Switch OFF, see Figure 11	25°C	2.7 V		0.2		nA
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO On leakage current	V_{NC} or V_{NO} = 2.3 V, V_{COM} = Open,	Switch ON, see Figure 12	25°C	2.7 V		2.8		nA
$I_{COM(ON)}$	COM On leakage current	V_{NC} or V_{NO} = 2.3 V or Open, V_{COM} = 2.3 V,	Switch ON, see Figure 12	25°C	2.7 V		0.47		nA
Digital Input (IN)									
V_{IH}	Input logic high			Full		1.8		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		Full	2.7 V	–1		1	µA
Dynamic									
t_{ON}	Turnon time	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, see Figure 14	25°C	2.3 V to 2.7 V		40	55	ns
				Full				70	
t_{OFF}	Turnoff time	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, see Figure 14	25°C	2.3 V to 2.7 V		30	40	ns
				Full				55	
t_{BBM}	Break-before-make time	$V_{NC} = V_{NO} = V_+ / 2$, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	2.3 V to 2.7 V	1	33	39	ns
				Full		1			
Q_C	Charge injection	C_L = 1 nF, V_{GEN} = 0 V,	See Figure 19	25°C	2.5 V		13		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or $V_{NO} = V_+$ or GND,	Switch OFF, see Figure 13	25°C	2.5 V		23		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or $V_{NO} = V_+$ or GND,	Switch ON, see Figure 13	25°C	2.5 V		84		pF
$C_{COM(ON)}$	COM ON capacitance	$V_{COM} = V_+$ or GND,	Switch ON, see Figure 13	25°C	2.5 V		84		pF
C_{IN}	Digital input capacitance	V_{IN} = V+ or GND,	See Figure 13	25°C	2.5 V		2.1		pF
BW	Bandwidth	R_L = 50 Ω,	Switch ON, see Figure 16	25°C	2.5 V		100		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see Figure 17	25°C	2.5 V		–64		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, see Figure 18	25°C	2.5 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, f = 600 Hz to 20 kHz,	C_L = 50 pF, see Figure 20	25°C	2.5 V		0.025%		
Supply									
I_+	Positive supply current	$V_{IN} = V_+$ or GND,	Switch ON or OFF	Full	2.7 V			0.1	µA

6.8 Electrical Characteristics for 1.8-V Supply

V_+ = 1.65 V to 1.95 V and T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP[(1)]	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}, V_{NC}	Analog signal					0		V_+	V
r_{peak}	Peak ON-resistance	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –2 mA,	Switch ON, see Figure 10	25°C	1.8 V		4	4.9	Ω
				Full				4.9	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 1.5 V, I_{COM} = –2 mA,	Switch ON, see Figure 10	25°C	1.8 V		1.7	3.2	Ω
				Full				3.2	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = –2 mA,	Switch ON, see Figure 10	25°C	1.8 V		0.7		Ω
				Full			0.7		
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –2 mA,	Switch ON, see Figure 10	25°C	1.8 V		1.85		Ω
				Full			1.85		
		V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = –2 mA,		25°C			0.9		
				Full			0.9		
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 1.65 V, V_{COM} = 0,	Switch OFF, see Figure 11	25°C	1.95 V		0.2		nA
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 1.65 V, V_{COM} = Open,	Switch ON, see Figure 12	25°C	1.95 V		2.8		nA
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = 1.65 V or open, V_{COM} = 1.65 V,	Switch ON, see Figure 12	25°C	1.95 V		0.47		nA
Digital Input (IN)									
V_{IH}	Input logic high			Full		1.5		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		Full	1.95 V	–1		1	μA
Dynamic									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 14	25°C	1.65 V to 1.95 V		65	70	ns
				Full				95	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 14	25°C	1.65 V to 1.95 V		40	55	ns
				Full				70	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+ / 2, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	1.65 V to 1.95 V	1	60	72	ns
				Full		0.5			
Q_C	Charge injection	C_L = 1 nF, V_{GEN} = 0 V,	See Figure 19	25°C	1.8 V		13		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V+ or GND,	Switch OFF, see Figure 13	25°C	1.8 V		23		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch ON, see Figure 13	25°C	1.8 V		84		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND,	Switch ON, see Figure 13	25°C	1.8 V		84		pF
C_{IN}	Digital input capacitance	V_{IN} = V_+ or GND,	See Figure 13	25°C	1.8 V		2.1		pF
BW	Bandwidth	R_L = 50 Ω,	Switch ON, see Figure 16	25°C	5.5 V		100		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see Figure 17	25°C	1.8 V		–63		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, see Figure 18	25°C	1.8 V		–63		dB

(1) T_A = 25°C.

Electrical Characteristics for 1.8-V Supply (continued)

V_+ = 1.65 V to 1.95 V and T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Supply									
I_+	Positive supply current	V_{IN} = V_+ or GND,	Switch ON or OFF	Full	1.8 V			0.1	µA

6.9 Switching Characteristics for 5-V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 14	25°C	4.5 V to 5.5 V		20	35	ns
				Full				40	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 14	25°C	4.5 V to 5.5 V		15	20	ns
				Full				35	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	4.5 V to 5.5 V	1	12	14.5	ns
				Full		1			

6.10 Switching Characteristics for 3.3-V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 14	25°C	3 V to 3.6 V		30	40	ns
				Full				55	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 14	25°C	3 V to 3.6 V		20	25	ns
				Full				40	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	3 V to 3.6 V	1	21	29	ns
				Full		1			

6.11 Switching Characteristics for 2.5-V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 14	25°C	2.3 V to 2.7 V		40	55	ns
				Full				70	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 14	25°C	2.3 V to 2.7 V		30	40	ns
				Full				55	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	2.3 V to 2.7 V	1	33	39	ns
				Full		1			

6.12 Switching Characteristics for 1.8-V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 14	25°C	1.65 V to 1.95 V		65	70	ns
				Full				95	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 14	25°C	1.65 V to 1.95 V		40	55	ns
				Full				70	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, see Figure 15	25°C	1.65 V to 1.95 V	1	60	72	ns
				Full		1			

6.13 Typical Characteristics

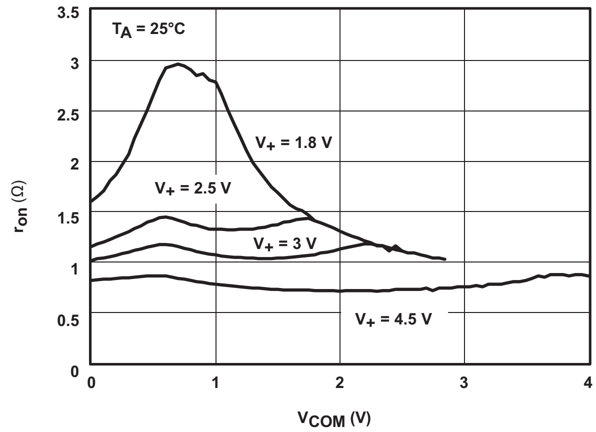


Figure 1. r_{on} vs V_{COM}

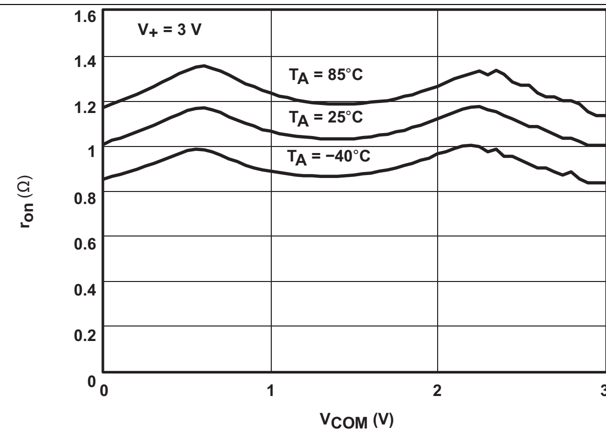


Figure 2. r_{on} vs V_{COM}

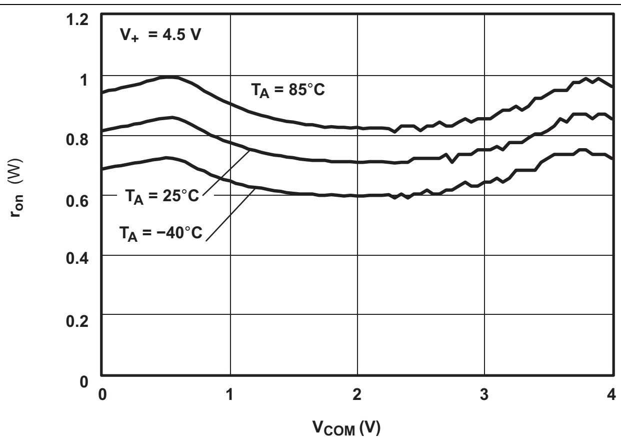


Figure 3. r_{on} vs V_{COM}

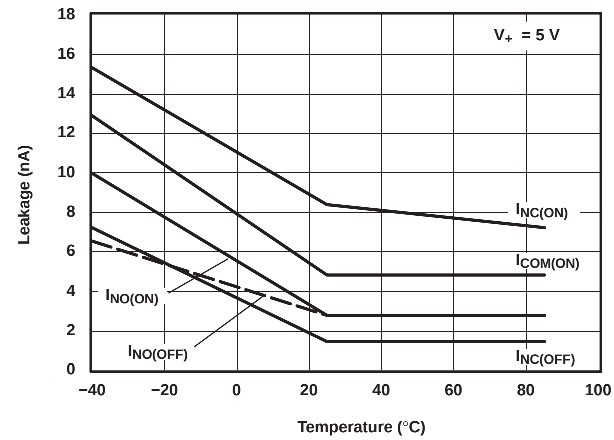


Figure 4. Leakage Current vs Temperature

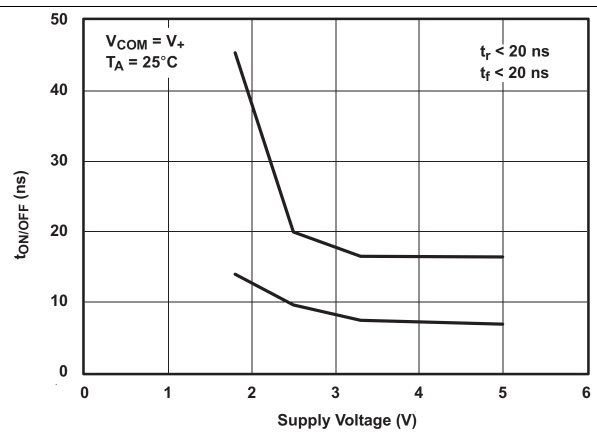


Figure 5. $t_{ON/OFF}$ vs V_+

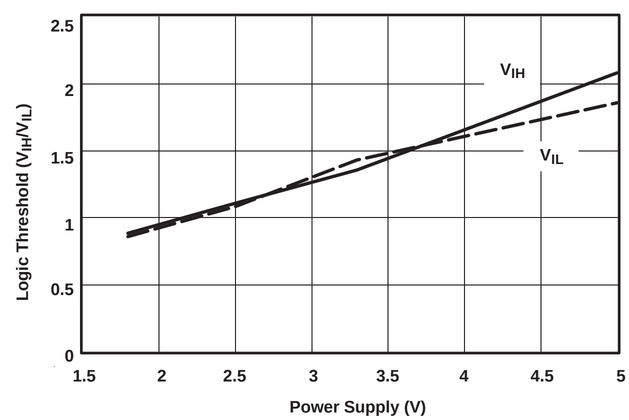


Figure 6. Logic Threshold vs Power Supply

Typical Characteristics (continued)

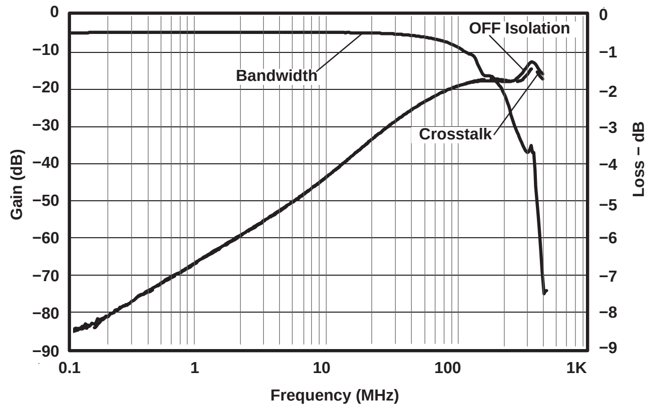


Figure 7. Frequency Response

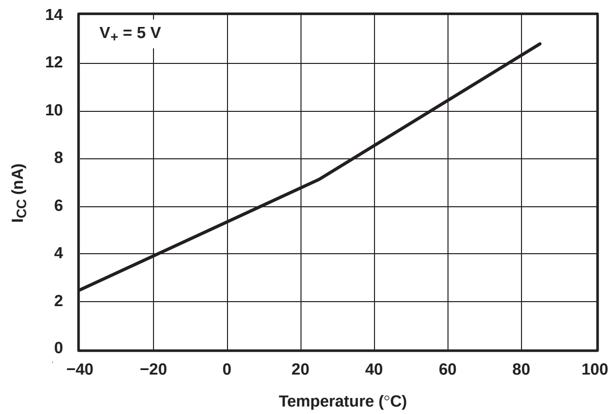


Figure 8. Power-Supply Current vs Temperature

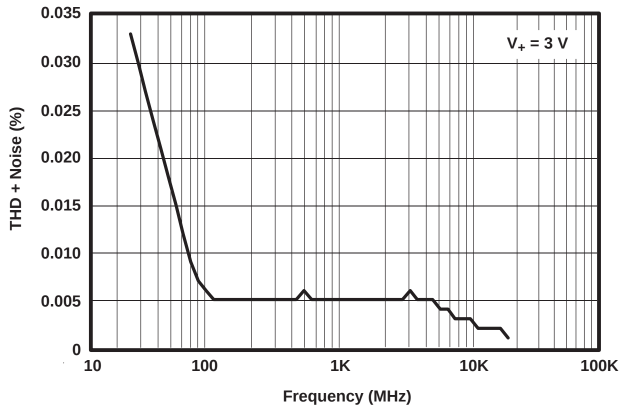


Figure 9. Total Harmonic Distortion (THD) vs Frequency

7 Parameter Measurement Information

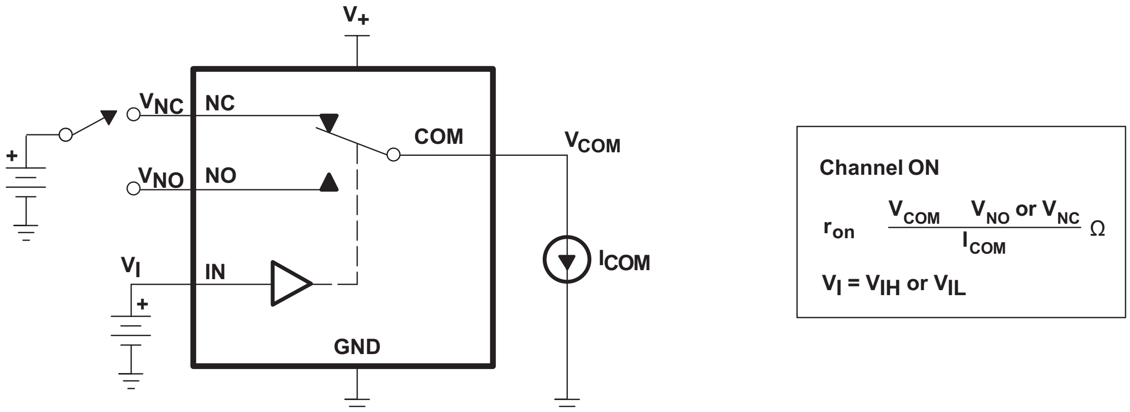


Figure 10. ON-State Resistance (r_{on})

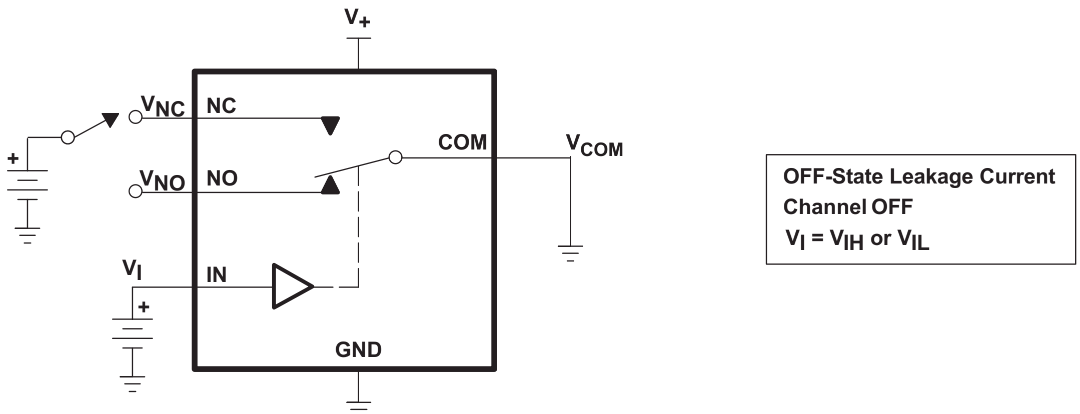


Figure 11. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NO(OFF)}$)

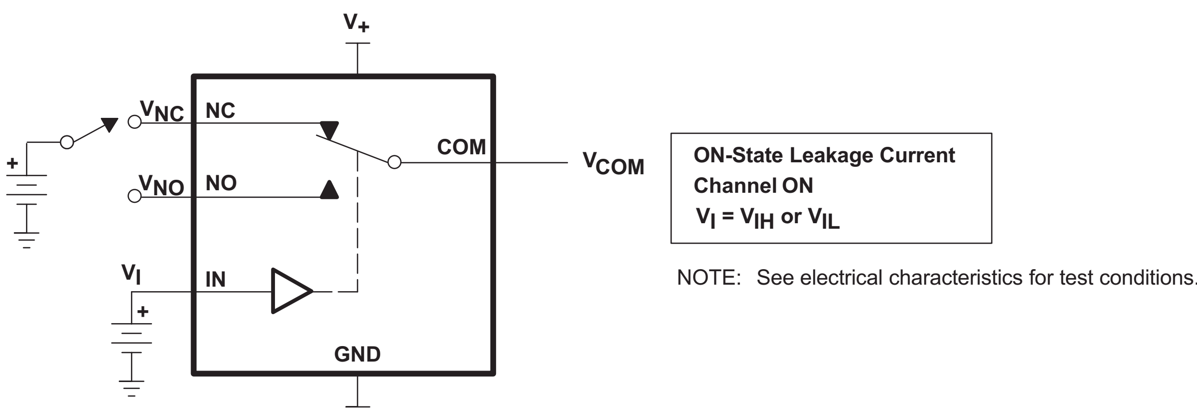


Figure 12. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

Parameter Measurement Information (continued)

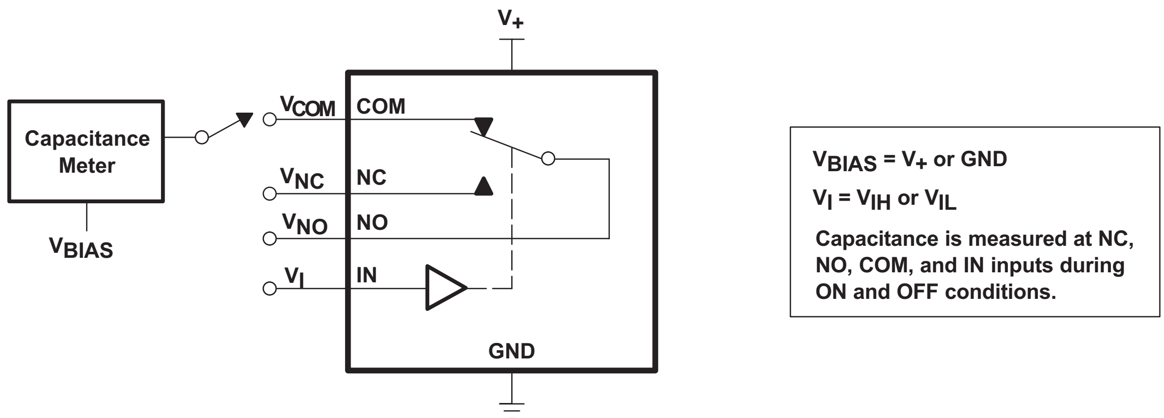
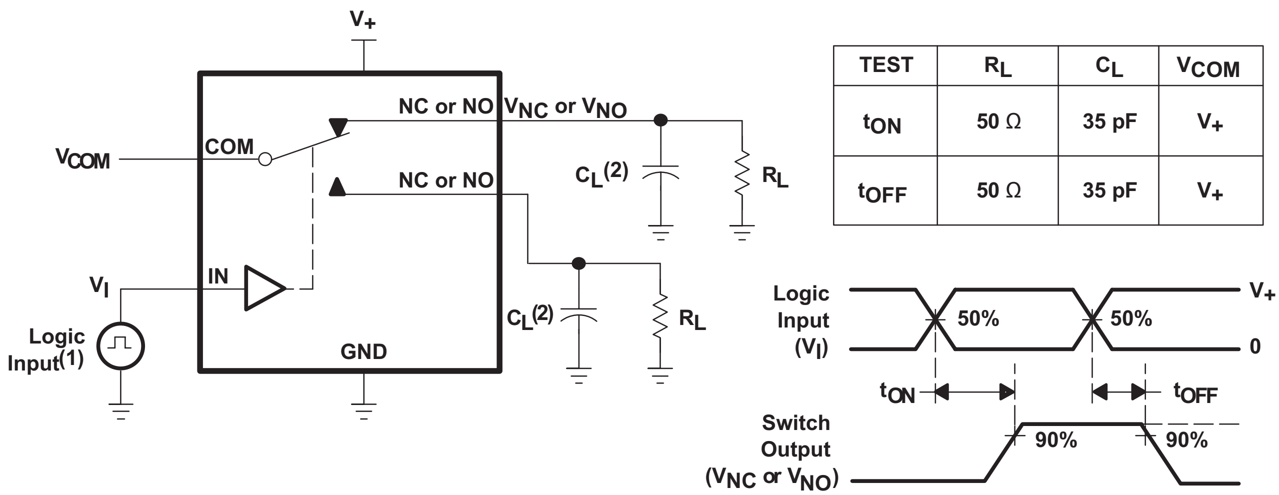


Figure 13. Capacitance (C_I, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



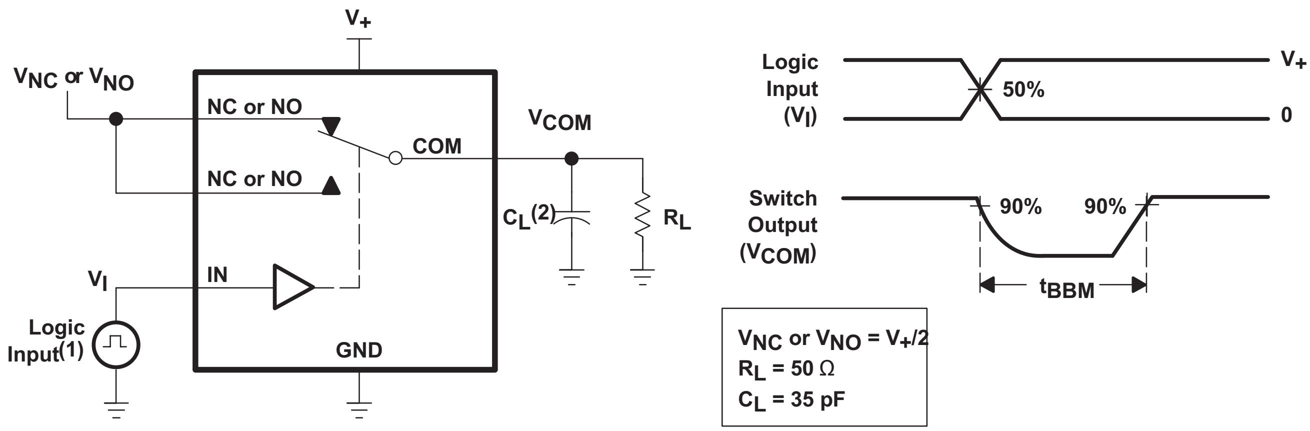
TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V+
t_{OFF}	50 Ω	35 pF	V+

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 14. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

Parameter Measurement Information (continued)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 15. Break-Before-Make Time (t_{BBM})

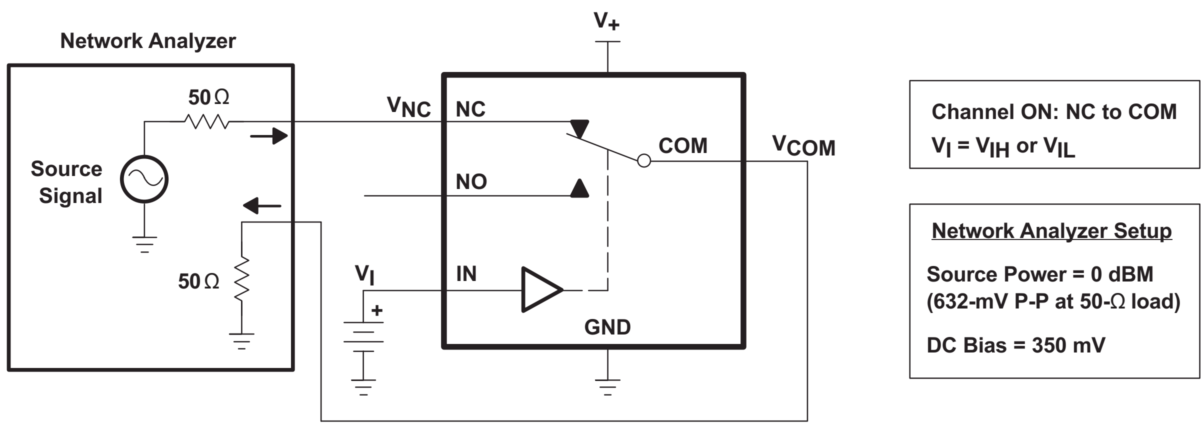


Figure 16. Bandwidth (BW)

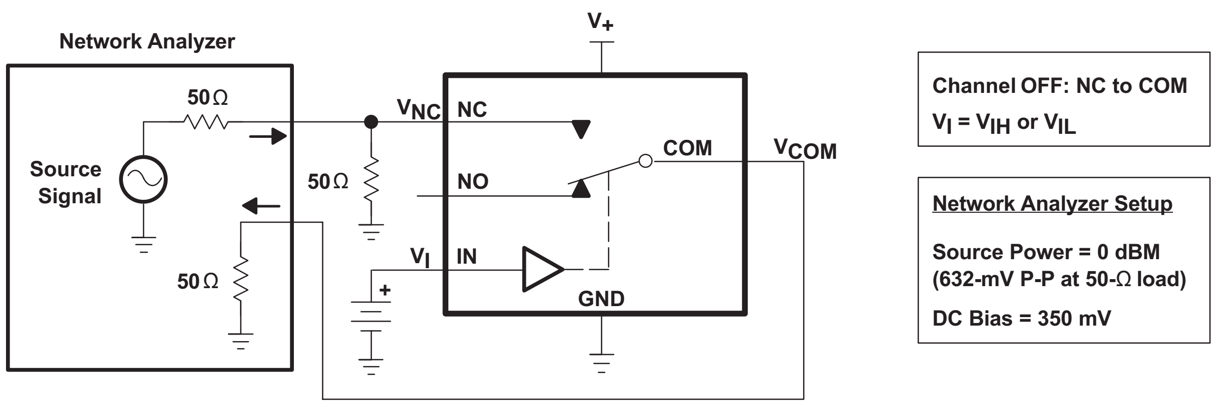


Figure 17. OFF Isolation (O_{ISO})

Parameter Measurement Information (continued)

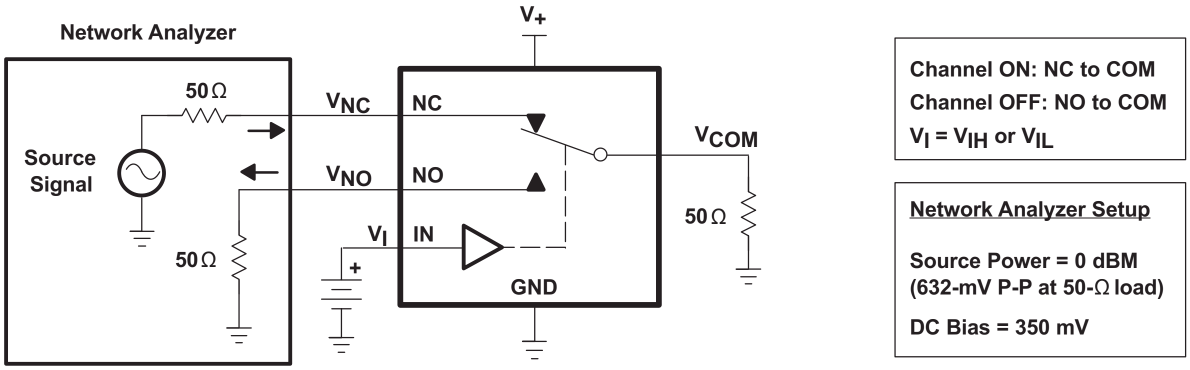
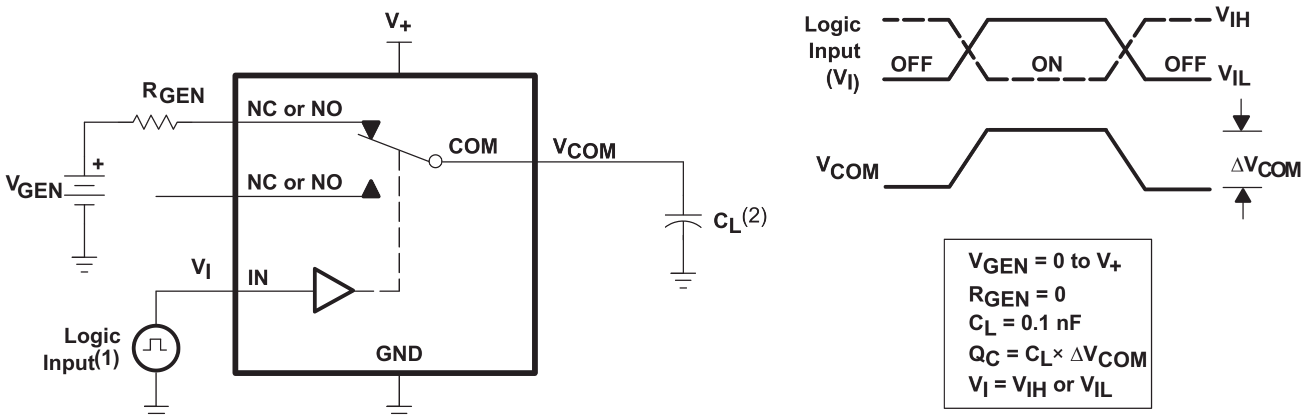


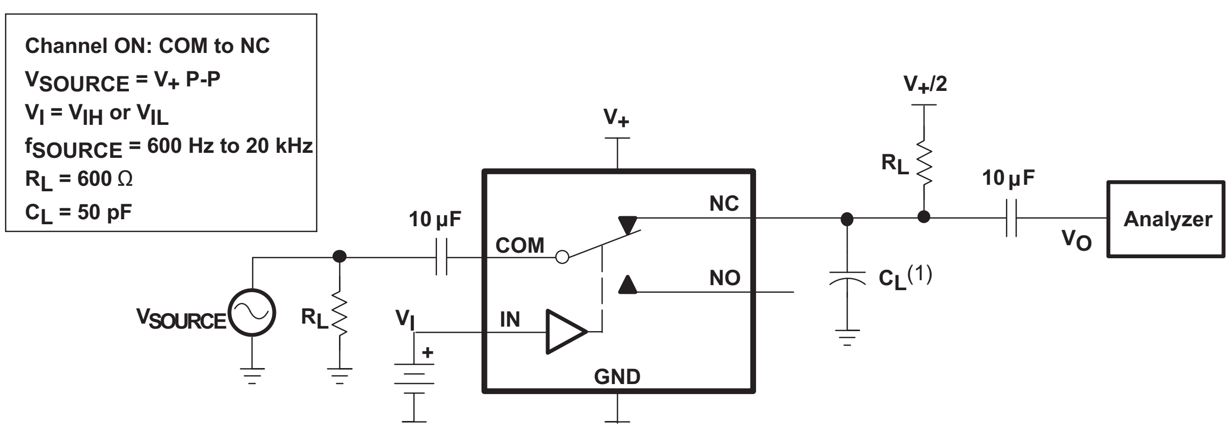
Figure 18. Crosstalk (X_{TALK})



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 19. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

Figure 20. Total Harmonic Distortion (THD)

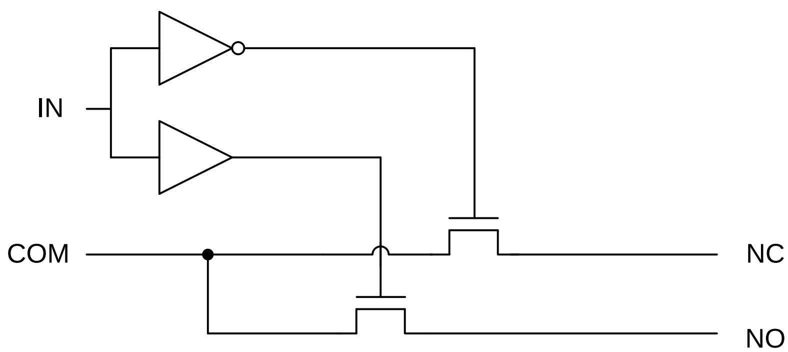
8 Detailed Description

8.1 Overview

The TS5A3159 is a single-pole-double-throw (SPDT) solid-state analog switch. The TS5A3159, like all analog switches, is bidirectional. When powered on, each COM pin is connected to the NC pin. For this device, NC stands for *normally closed* and NO stands for *normally open*. If IN is low, COM is connected to NC. If IN is high, COM is connected to NO.

The TS5A3159 is a break-before-make switch. This means that during switching, a connection is broken before a new connection is established. The NC and NO pins are never connected to each other.

8.2 Functional Block Diagram



8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A3159 make this switch an excellent choice for analog signals that require minimal distortion. In addition, the low THD allows audio signals to be preserved more clearly as they pass through the device.

The 1.65-V to 5.5-V operation allows compatibility with more logic levels, and the bidirectional I/Os can pass analog signals from 0 V to V_+ with low distortion.

8.4 Device Functional Modes

Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A3159 can be used in a variety of customer systems. The TS5A3159 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

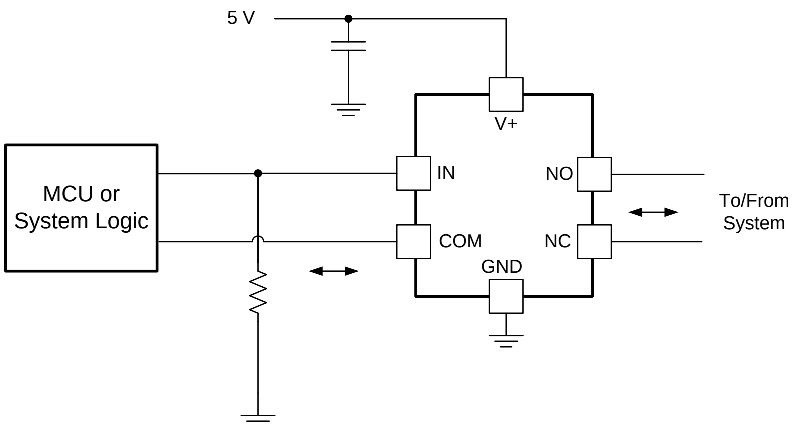


Figure 21. System Schematic for TS5A3159

9.2.1 Design Requirements

In this particular application, V_+ was 1.8 V, although V_+ is allowed to be any voltage specified in *Recommended Operating Conditions*. A decoupling capacitor is recommended on the V+ pin. See *Power Supply Recommendations* for more details.

9.2.2 Detailed Design Procedure

In this application, IN is, by default, pulled low to GND. Choose the resistor size based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

9.2.3 Application Curve

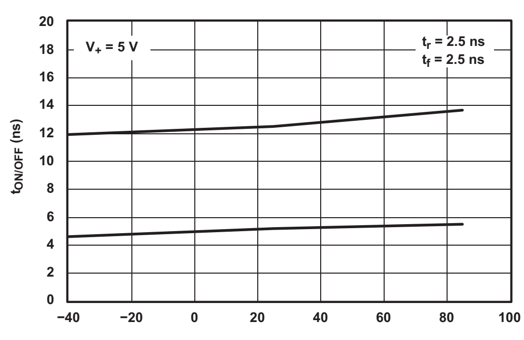


Figure 22. $t_{ON/OFF}$ vs Temperature

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-μF or 0.022-μF capacitor is recommended for each V_{CC} because the VCC pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN pin must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states.

11.2 Layout Example

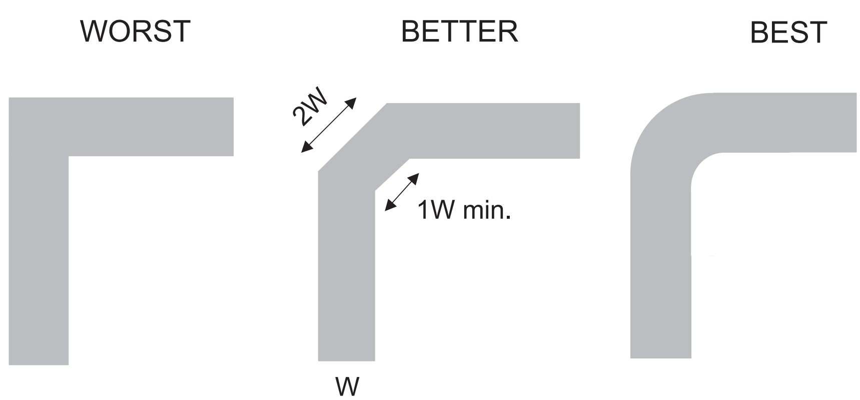


Figure 23. Trace Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

Table 2. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
r_{peak}	Peak ON-state resistance over a specified voltage range
Δr_{on}	Difference of r_{on} between channels
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) being open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) being open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) being open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Minimum input voltage for logic low for the control input (IN)
V_{IN}	Voltage at IN
I_{IH}, I_{IL}	Leakage current measured at IN
t_{ON}	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal, and analog outputs (COM, NC, or NO) signal when the switch is turning ON.
t_{OFF}	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal, and analog outputs (COM, NC, or NO) signal when the switch is turning OFF.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO), when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_O$, C_L is the load capacitance, and ΔV_O is the change in analog output voltage.

Table 2. Parameter Description (continued)

SYMBOL	DESCRIPTION
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C_{IN}	Capacitance of IN
O_{ISO}	OFF isolation of the switch is a measurement OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
I_+	Static power-supply current with the control (IN) terminal at V_+ or GND
ΔI_+	This is the increase in I_+ for each control (IN) input that is at the specified voltage, rather than at V_+ or GND.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- *Implications of Slow or Floating CMOS Inputs*, SCBA004

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A3159DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JA8K ~ JA8R)	Samples
TS5A3159DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JA8K ~ JA8R)	Samples
TS5A3159DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JA8K ~ JA8R)	Samples
TS5A3159DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JA8K ~ JA8R)	Samples
TS5A3159DBVTE4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JA8K ~ JA8R)	Samples
TS5A3159DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JA8K ~ JA8R)	Samples
TS5A3159DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JAK ~ JAR ~ JAZ)	Samples
TS5A3159DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JAK ~ JAR ~ JAZ)	Samples
TS5A3159DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JAK ~ JAR ~ JAZ)	Samples
TS5A3159DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JAK ~ JAR ~ JAZ)	Samples
TS5A3159DCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JAK ~ JAR ~ JAZ)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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OTHER QUALIFIED VERSIONS OF TS5A3159 :

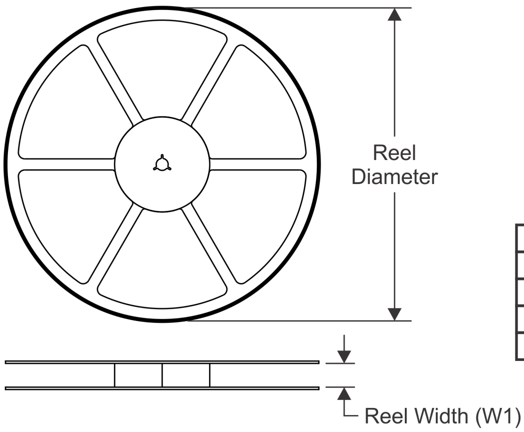
- Automotive: TS5A3159-Q1
- Enhanced Product: TS5A3159-EP

NOTE: Qualified Version Definitions:

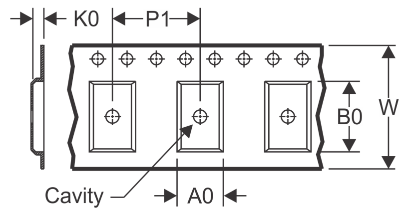
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

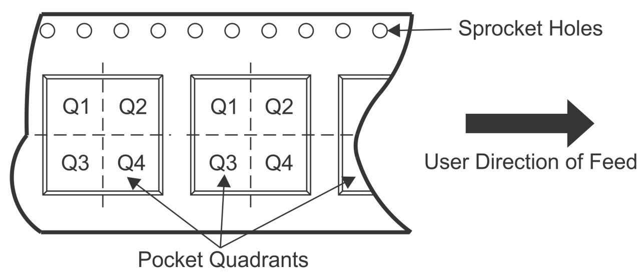


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

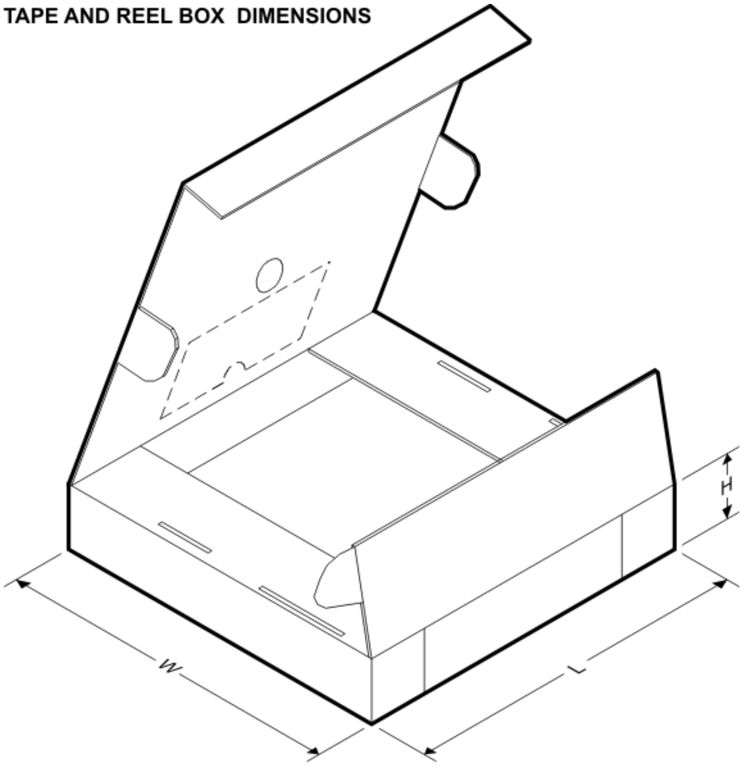
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3159DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3159DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3159DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TS5A3159DCKR	SC70	DCK	6	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
TS5A3159DCKT	SC70	DCK	6	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
TS5A3159DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3

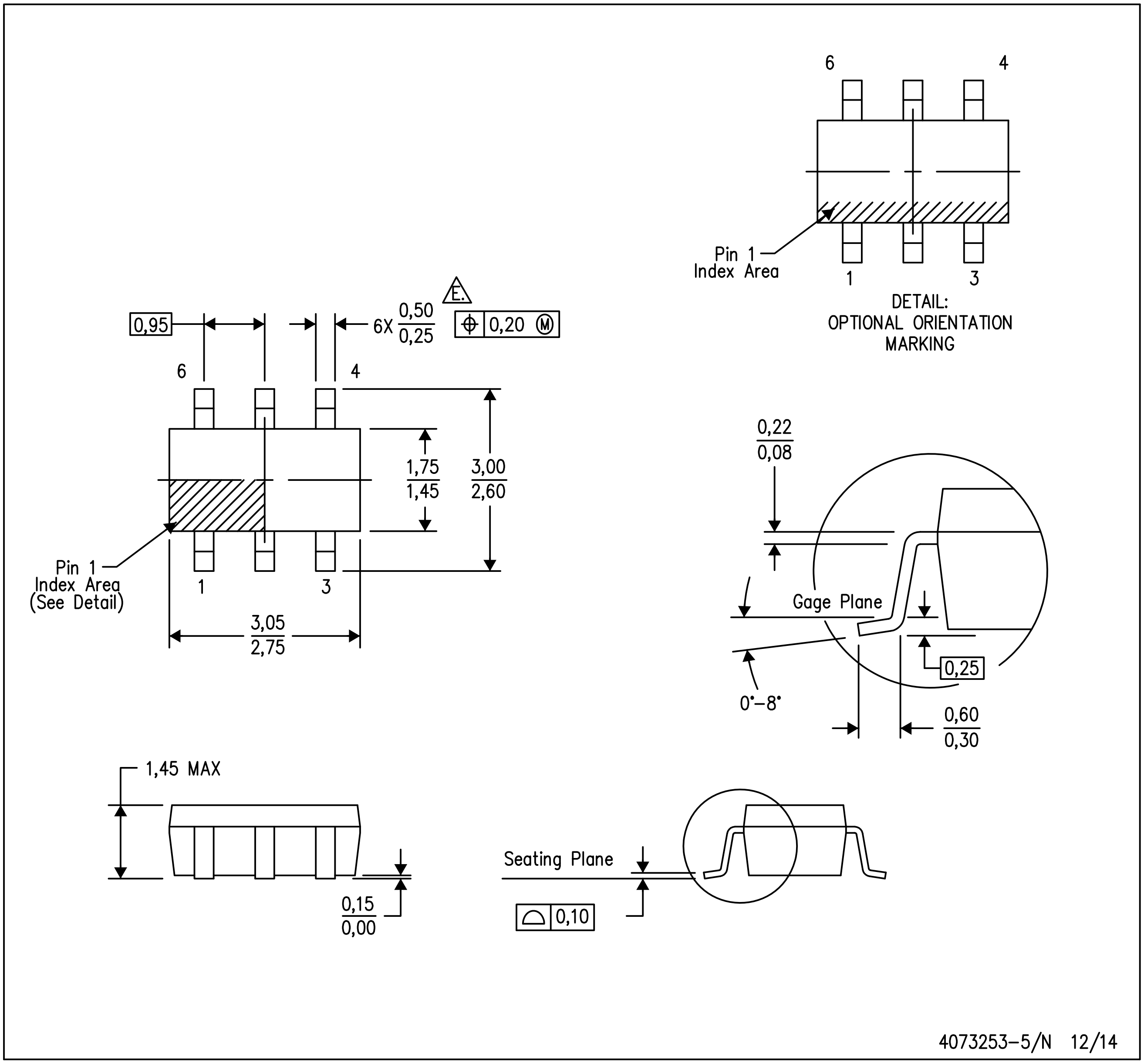
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

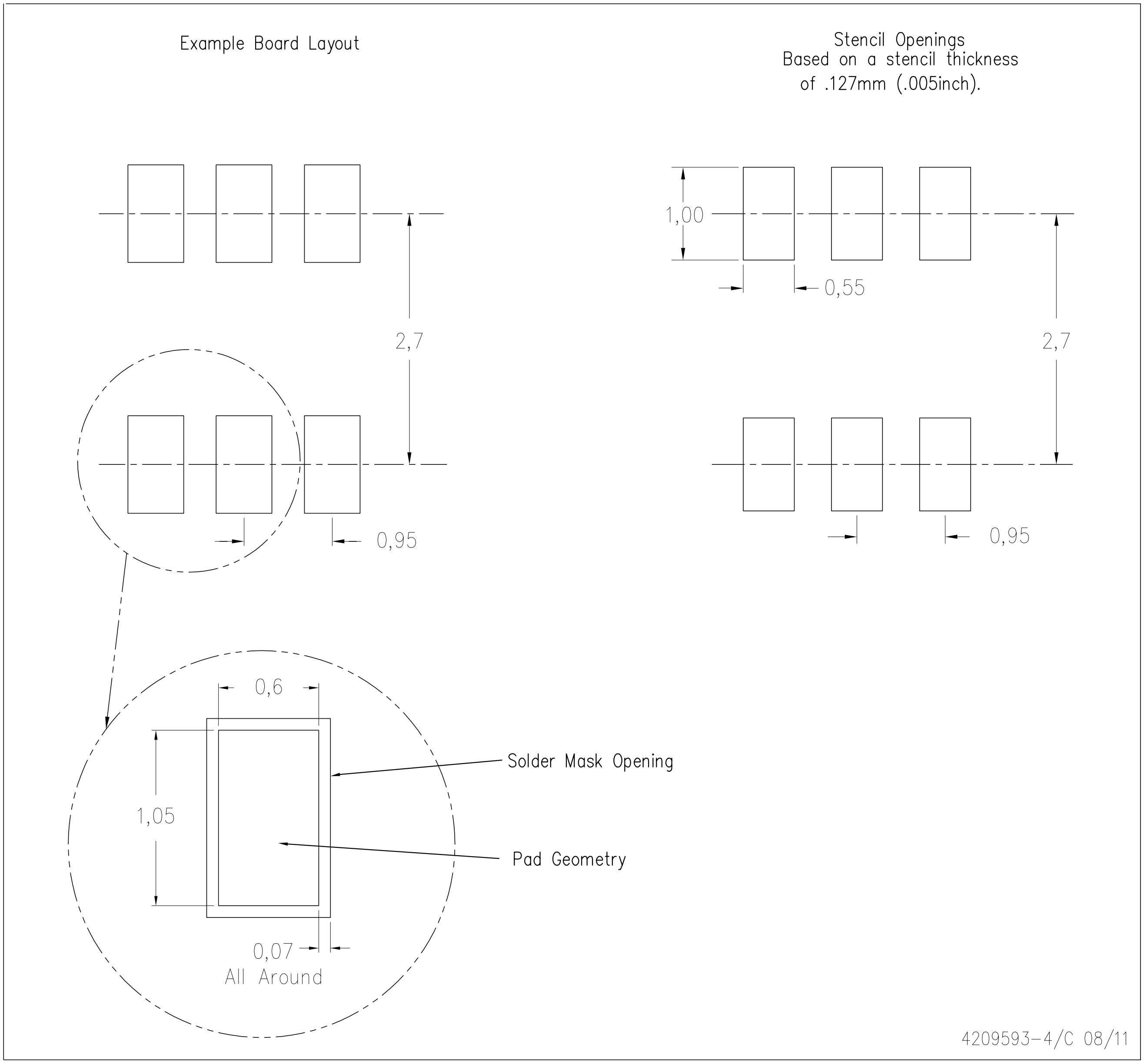
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3159DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
TS5A3159DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
TS5A3159DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
TS5A3159DCKR	SC70	DCK	6	3000	205.0	200.0	33.0
TS5A3159DCKT	SC70	DCK	6	250	205.0	200.0	33.0
TS5A3159DCKT	SC70	DCK	6	250	202.0	201.0	28.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



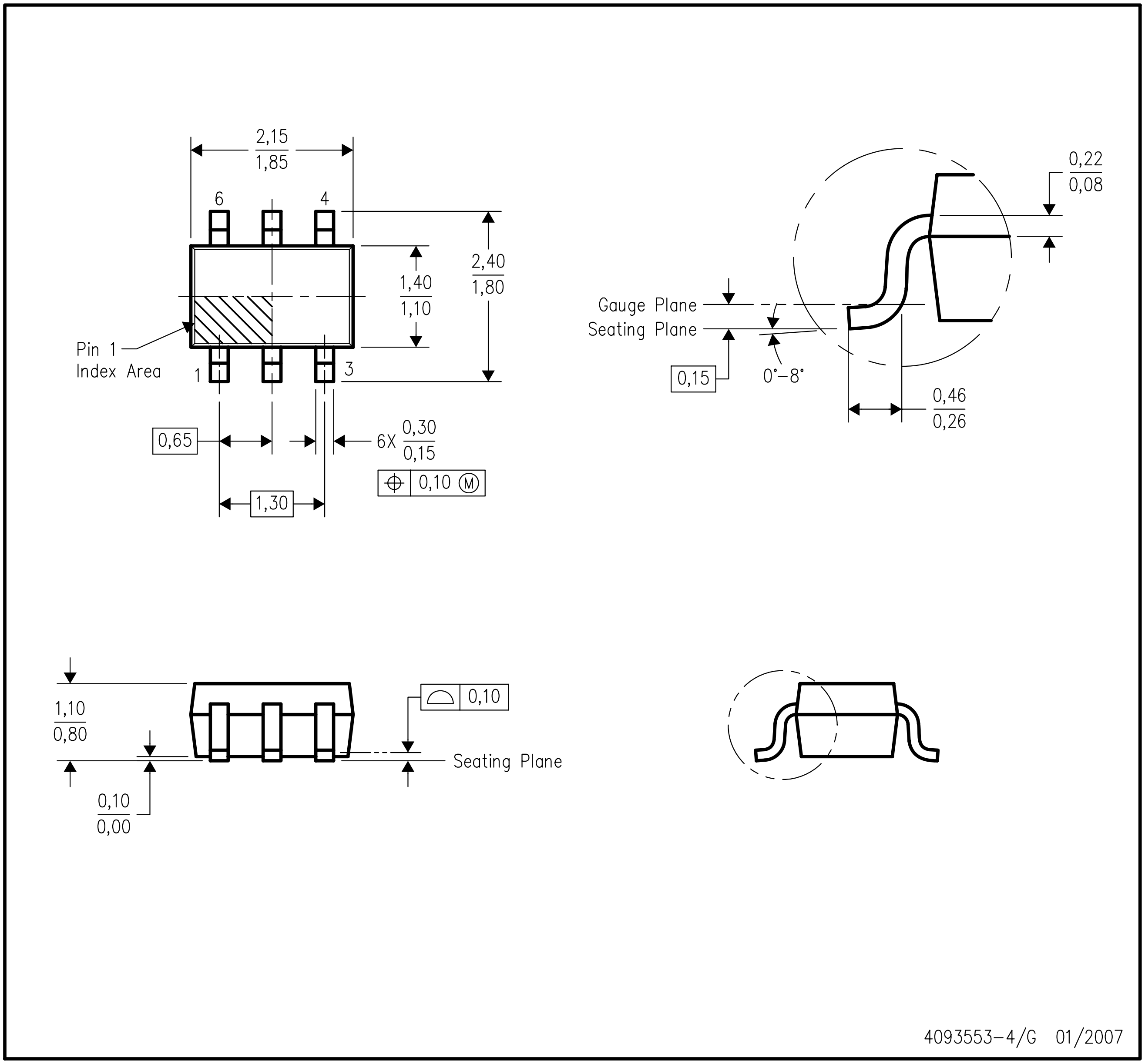
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6) PLASTIC SMALL OUTLINE



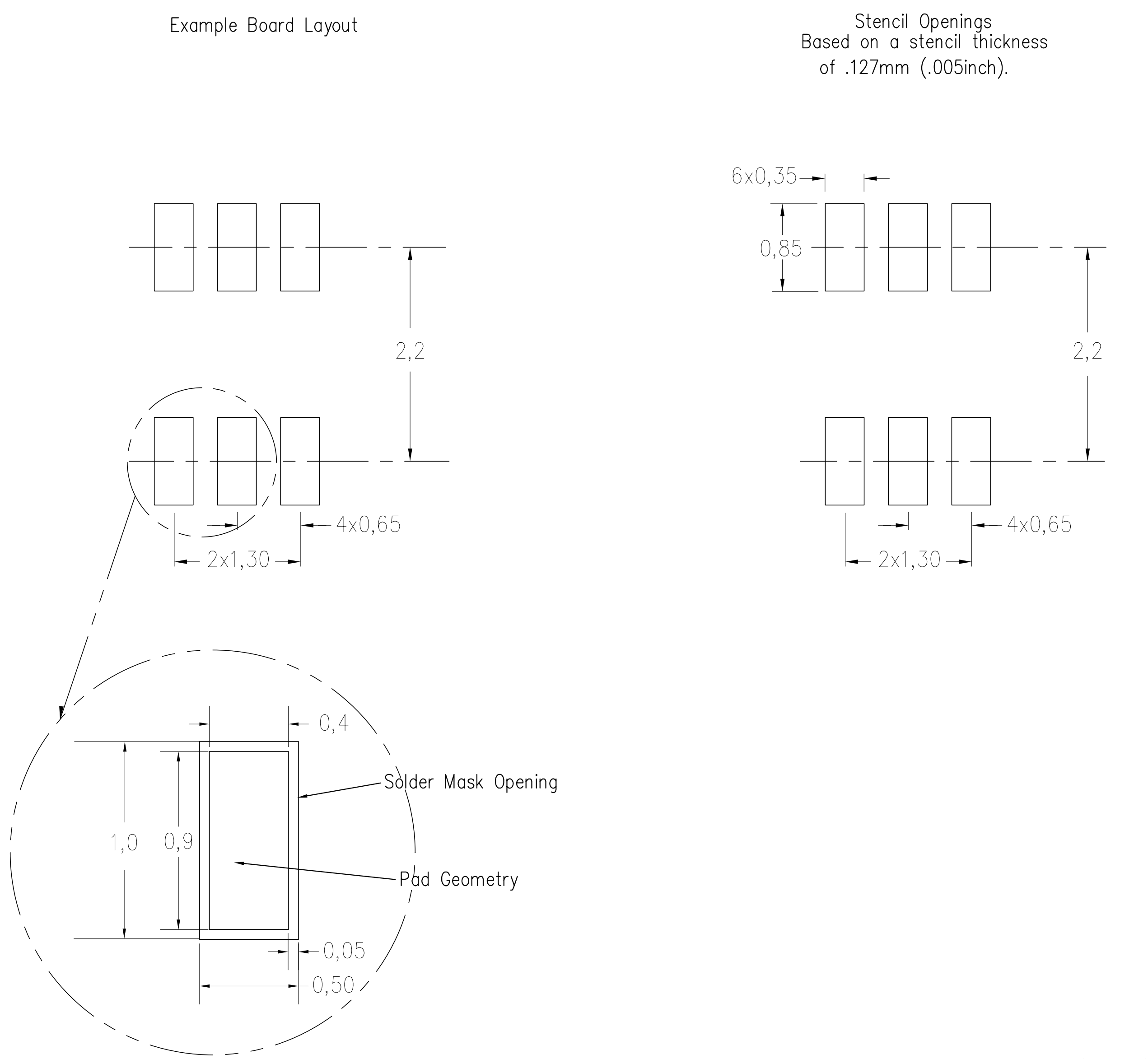
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.